Thomas SARNO

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France

29 years old
French driving license
French nationality

Hardware Security Engineer, PhD

Skills:

Conception **:**
- VHDL Verilog
- FPGA (Xillinx ISE/Vivado)
- Simulation (ModelSim)
- Conception PCB

Security**:**
- **Fault injection** (eg. EM pulse attack)
- **Hardware Cryptanalysis** (eg. DFA, CPA)
- **Testbench setup** for Fault injection/Side channel

Script/Data analysis:
- Perl Python
- Matlab

Programming:
- C/C++ Java
- Labview/Labview ARM

Others:
- LaTex

Languages:

- French : native language
- **English : fluent**
  TOEIC 975/990
  TOEFL 105/125
- **Chinese (mandarin) : conversation**
  6 months in Shanghai
- Spanish : working knowledge

Others:

- **Labs VHDL**, 1st year Master's degree, 2015

Working Experience:

Harware Security Engineer (2016) – *1 Year :*
Aix-Marseille University – IM2NP department
References : Romain Wacquez (CEA-Tech), Bruno Robisson (CEA-Tech), Edith Kussener (ISEN)

- Test of chaotic EM generator counter-measure against cryptanalysis attacks
- **Side-channel attacks** on **hardware** and **software** cryptographic algorithm
- EM cryptanalysis tools development (synchronization, filtering, …)
- Participation to the "RESET" project

Hardware Security Engineer (2012-2015) – *3 Years :*
Crocus Technology
References : Assia Tria (CEA-Tech), Bruno Mussard and Ali Alaoui (Crocus Technology)

- Theoretical analysis of spintronic memory weaknesses
- Fault attack **testbench development** and setup
- **Physical fault attacks** (electromagnetic pulse attacks, static magnetic field perturbations) of MRAM chips
- **EM side channel analysis** of MRAM chips
- Countermeasures design
- Participation to the **ANR project** "SESAME"
- **PhD** received

Analog Design Engineer (2011) – *6 Months*:
*Internship, at **Shanghai Jiaotong University** – China*

-Large bandwith (700 MHz) PLL design and simulation
-TSMC 0,18 µm technology

Education:

2012-2015
PhD in microelectronics at Crocus Technology :
Secure characterization of magnetic memories MRAM

2008-2011
"Diplôme d'ingénieur" Mines de Saint Etienne – ISMIN
Mines de St Étienne in top 15 French graduate engineering schools
Major : Microelectronics design

2010-2011
Research master's degree - Aix-Marseille University
Major : Micro et nanotechnologies

Hobbies:

- Sport : Ski, hiking
- Associations : Vice-president of « Ingénieur Sans Frontières » (2010), Gardanne antenna
- Music *:* Piano, 8 years
- Electronics/Programming : connected weather station (Raspberry Pi), music streaming homemade platform, self balanced robot